ELECTRONIC MATERIALS
Precursor for Chapter 6 of Prof. Kasap’s Book
Electrical Properties of Materials

This Material is an over view of Fundamentals, Devices, and Processing. Excellent Overview (but in less details as compared to Dr. Kasap’s Detailed Book –by design) gives you a Big Picture.

Text: Foundations of Materials Science and Engineering
FIGURE 13.29 (a) \textit{pn} junction diode showing majority carriers (holes in \textit{p-type} material and electrons in \textit{n-type} material) diffusing toward junction. (b) Formation of depletion region at and near \textit{pn} junction due to loss of majority carriers in this region by recombination. Only ions remain in this region in their positions in the crystal structure.
Current –Voltage Characteristics

Forward and Reverse Bias Mixed (Ideally there should not be a leakage current but it unavoidable to thermal jumping

FIGURE 13.31 Schematic of current-voltage characteristics of a pn junction diode. When the pn junction diode is reversed-biased, a leakage current due to minority carriers combining exists. When the pn junction diode is forward-biased, a large current flows due to recombination of majority carriers.
Rectifying Effect shown from AC to DC

From William Smith’s Book

Diagram illustrating the rectifying action of a pn junction diode to convert alternating current (ac) to direct current (dc). The output current is not completely direct current but is mostly positive. This ac signal can be smoothed out by using other electronic devices.
pnp junction Transistor – Thin layer of p in the middle called Base
Bipolar n p n Transistor
On a Si single crystal

**FIGURE 13.39** Microelectronic planar bipolar *n*p*n* transistor fabricated in a single crystal of silicon by a series of operations that require access to only one surface of the silicon chip. The entire chip is doped with *p*-type impurities, then islands of *n*-type silicon are formed. Smaller *p*- and *n*-type areas are next created within these islands in order to define the three fundamental elements of the transistor: the emitter, the base, and the collector. In this microelectronic bipolar transistor the emitter-base junction is forward-biased and the collector-base junction is reverse-biased, as in the case of the isolated *n*p*n* transistor of Fig. 13.36. The device exhibits gain because a small signal applied to the base can control a large one at the collector. (After J. D. Meindl, Microelectronic Circuit Elements, Sci. Am., September 1977, p. 75. Copyright © Scientific American Inc. All rights reserved.)
FIGURE 13.45 Selective doping processes for exposed silicon surfaces: (a) high-temperature diffusion of impurity atoms; (b) ion implantation. (After S. Triebwasser, “Today and Tomorrow in Microelectronics,” from the Proceedings of an NSF workshop held at Arlie, Va., Nov. 19–22, 1978.)
**FIGURE 13.28** (a) pn junction diode grown in the form of a single crystal bar. (b) Planar pn junction formed by selectively diffusing a p-type impurity into an n-type semiconductor crystal.

**FIGURE 13.30** Reverse-biased pn junction diode. Majority carriers are attracted away from the junction, creating a wider depletion region than when the junction is at equilibrium. Current flow due to majority carriers is reduced to near zero. However, minority carriers are biased forward, creating a small leakage current, as shown in Fig. 5.31.
**p-n junction with potential**

**Forward Bias**

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**FIGURE 13.32** Forward-biased $pn$ junction diode. Majority carriers are repelled toward the junction and cross over it to recombine so that a large current flows.
Zener Diode

Uses this Breakdown Voltage to Rectifier

FIGURE 13.35 Zener (avalanche) diode characteristic curve. A large reverse current is produced at the breakdown-voltage region.
FIGURE 13.37 Charge carrier motion during the normal operation of an npn transistor. Most of the current consists of electrons from the emitter which go right through the base to the collector. Some of the electrons, about 1 to 5 percent, recombine with holes from the base current flow. Small reverse currents due to thermally generated carriers are also present, as indicated. (After R. J. Smith, "Currents, Devices and Systems," 3d ed., Wiley, 1976, p. 343.)
Fabrication Process – Step No. 1- Drawing of the layout of the FET's Transistors etc.
**Deposition of SiO\textsubscript{2} (MO)**

1. **Glass Mask**
   - Photoresist Before UV Radiation
   - SiO\textsubscript{2} - White areas
   - Note removal of SiO\textsubscript{2} layer in the middle picture

2. **Deposition of Metals**
   - Photoresist
   - Si crystal
   - Exposed Photoresist
   - Remove White Area
   - Unexposed Resist - Next
   - 1. Exposed Resist Remains
   - 2. Deposit Metal on resist – We want the metal directly on Si in midsection (arrow down) to remain, rest should be removed.
   - 3. Final metal layer is shown on right

3. **Glass Plate Mask**
   - Ultraviolet Radiation
   - Photoresist After UV Radiation
   - Si\textsubscript{3}N\textsubscript{4}
   - O\textsubscript{2}
   - SiO\textsubscript{2}
   - 2H\textsubscript{2}
   - 3SiH\textsubscript{4}
   - 4NH\textsubscript{3}
   - Si\textsubscript{3}N\textsubscript{4}
   - 12H\textsubscript{2}
   - **Objective is Deposit metal layer of a particular Shape on Si Crystal - L-shaped**

**Ion Implantation (Top) & Diffusion Drive In Process (Bottom) Shown below:**

These layers may be deposited between 200\textdegree{} and 450\textdegree{} using CVD.

**Processes shown below:**

- SiH\textsubscript{4} + O\textsubscript{2} + SiO\textsubscript{2} + 2H\textsubscript{2}
- 3SiH\textsubscript{4} + 4NH\textsubscript{3} + Si\textsubscript{3}N\textsubscript{4} + 12H\textsubscript{2}
Entire Chip Making Process shown here but we are going to look at this Step by Step in the following Slides.
I. CVD Si₃N₄ over entire area of Wafer

II. Photolithography shown on the left defines the area of transistors and MOS (integrated Circuit).

III. The Si₃N₄ layer is removed in the areas where are no transistors by chemical etching.

IV. film defines areas for formation of Transistors-Si₃N₄

V. p-regions deposited, SiO₂ is grown Internally

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**STEP No. 1**

1. CVD Si₃N₄ over entire area of Wafer
2. Photolithography shown on the left defines the area of transistors and MOS (integrated Circuit).
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4. film defines areas for formation of Transistors-Si₃N₄
5. p-regions deposited, SiO₂ is grown Internally
Step No. 2

Si₃N₄ is removed by selective etching and typically SiO₂. Creates areas metallic contact on top (electrically isolated by this insulator).
I. CVD Si3N4 film defines areas for formation of Transistors-SiN, p-regions deposited, SiO2@ grown internally.

II. SiN Layer removed by Enchant that does not attack the SiO2. a clean SiO2 grown by heating in air and then poly Si deposited.

III. Deposition SiO2 by CVD process

Creates new areas for transistor contacts between SiO2.

IV. Metal Contact

STEP NO.3 & 4

1st. Mask SiN Deposition

2nd Mask-PolySi Gate

3rd. Mask- Deposited Insulators

4th.. Mask-Metal Contact areas
The rest of the Process

- Grow Gate Oxide
- Deposit Polysilicon
- Polysilicon Gate Definition
- n-drain Diffusion
- Deposit SiO₂
- Contact Areas
- Deposit Al
- Metal Definition
- Mask No.5 Expose Bonding pads
- Protective Passivation
- Wafer Probe
- Die (FET or Trans. Assembly) Separation
- Attach Die
- Wire Deposit
- Final product

Small Pieces are cut to Be placed in the Bakelite casing

Bakelite Casing-Black
Entire Chip Making Process shown here but we are going to look at this Step by Step in the following Slides.
FIGURE 13.48

CMOS FET has both n and p type in one FET
II-V and II-VII Semiconductors Commonly Used in Industry

**FIGURE 13.49** Part of the periodic table containing elements used in the formation of MX-type III–V and II–VI semiconductor compounds.
GaAs Semiconductors MEFET's (Metal Semiconductor FET)
Better Radiation resistance – Used in Military and Space application
Lot of Defects, and very expensive, Microwave Circuits, Direct band Gap (1.47 eV)
Leading higher mobilities $\mu_e = 0.72 \text{ m}^2/\text{v.s}$ (Si=0.135)

Next, we go to chapter 6 from Kasap’s Book